In the Claims:

The claims are as follows:

1 - 16 (Canceled)

17. (Currently Amended) A method for forming a semiconductor apparatus comprising the steps of:

forming an N+ diffusion and a P+ diffusion;

forming a polysilicon line, the polysilicon line having a P+ region and an N+ region, the polysilicon line having an N+/P+ junction area wherein said junction area comprises the area where the P+ region of the polysilicon line and the N+ region of the polysilicon line abut each other; and,

selectively forming a silicide strap over a portion of a top surface of the N+ region and the P+ region and extending across the junction area, wherein the silicide strap forms an electrical connection between the P+ region of the polysilicon line and the N+ region of the polysilicon line, and wherein the portion of the top surface of the N+ region and the P+ region does not comprise an entire top surface of the N+ region and the P+ region; and

selectively preventing the formation of silicide on the N+ diffusion and the P+ diffusion.

18. (Original) The method of claim 17 wherein the step of selectively forming a silicide strap comprises:

forming a hard mask on the semiconductor structure;

patterning the hard mask to expose the N+/P+ junction area; and

forming silicide in the exposed N+/P+ junction area.

19. (Original) The method of claim 17 wherein the step of selectively preventing the formation of silicide on the N+ diffusion and the P+ diffusion comprises:

forming a hard mask on the semiconductor structure; and

patterning the hard mask to expose portions of the semiconductor structure, said patterning not exposing the N+ diffusion and the P+ diffusion.

20. (Original) The method of claim 17 further comprising the step of:

completing devices and back end of line processes.

21. (Original) The method of claim 17 wherein the semiconductor structure is part of an SRAM.

22. (Original) The method of claim 17 wherein current leakage is reduced by selectively preventing silicide formation on the N+ diffusion and P+ diffusion.

23. (Original) The method of claim 22 wherein the current leakage reduced comprises Gate Induced Drain Leakage (GIDL).